CLAIMS

What is claimed is:

1. A method to configure a multi-port device comprising:

defining a first plurality of pointers, one pointer for each of a plurality of ports of the multi-port device; and

storing the first plurality of pointers in one or more capability structures of the multi-port device.

2. The method of claim 1, further comprising coupling the one or more capability structures with a second plurality of pointers.

3. The method of claim 2, wherein the second plurality of pointers comprise relative pointers.

4. The method of claim 1, further comprising:

storing a plurality of programmable elements representing a plurality of capabilities in a plurality of capability structures, wherein the programmable elements are organized according to capability; and

pointing each of the first plurality of pointers to one of the plurality of capability structures.

5. The method of claim 4, further comprising pointing two of the first plurality of pointers corresponding to two of the plurality of ports to one of the plurality of capability structures if the two ports support the same capability.

6. The method of claim 1, wherein the multi-port device is an Advance Switching component.

7. A machine-readable medium that provides instructions that, if executed by a processor, will cause the processor to perform operations to configure a multi-port device, the operations comprising:

defining a first plurality of pointers, one pointer for each of a plurality of ports of the multi-port device; and

storing the first plurality of pointers in one or more capability structures of the multi-port device.

8. The machine-readable medium of claim 7, wherein the method further comprises coupling the one or more capability structures with a second plurality of pointers.

9. The machine-readable medium of claim 8, wherein the second plurality of pointers comprise relative pointers.

10. The machine-readable medium of claim 7, wherein the method further comprises:

storing a plurality of programmable elements representing a plurality of capabilities in a plurality of capability structures, wherein the programmable elements are organized according to capability; and

pointing each of the first plurality of pointers to one of the plurality of capability structures.

11. The machine-readable medium of claim 7, wherein the multi-port device is an Advance Switching component.

12. An apparatus comprising:

a plurality of ports; and

a storage device to store one or more capability structures, wherein the one or more capability structures store a first plurality of pointers, one pointer for each of the plurality of ports.

13. The apparatus of claim 12, wherein the one or more capability structures are coupled to each other via a second plurality of pointers.

14. The apparatus of claim 13, wherein the second plurality of pointers comprise relative pointers.

15. The apparatus of claim 12, wherein the storage device further stores a second plurality of capability structures to store a plurality of programmable elements

representing a plurality of capabilities, the plurality of programmable elements are organized according to capability, and each of the first plurality of pointers is pointed to one of the second plurality of capability structures.

16. The apparatus of claim 15, wherein two of the first plurality of pointers corresponding to two of the plurality of ports are pointed to one of the second plurality of capability structures if the two ports support the same capability.

17. The apparatus of claim 12, wherein the plurality of ports includes one or more Advance Switching ports.

18. A computer system comprising:

a graphics chip; and

a multi-port device coupled to the graphics chip, the multi-port device comprising

a plurality of ports; and

a storage device to store one or more capability structures, wherein the plurality of capability structures store a first plurality of pointers, one pointer for each of the plurality of ports.

19. The computer system of claim 18, wherein the one or more capability structures are coupled to each other via a second plurality of pointers.

20. The computer system of claim 19, wherein the second plurality of pointers comprise relative pointers.

21. The computer system of claim 18, wherein the storage device further stores a second plurality of capability structures to store a plurality of programmable elements representing a plurality of capabilities, the plurality of programmable elements are organized according to capability, and each of the first plurality of pointers is pointed to one of the second plurality of capability structures.

22. The computer system of claim 21, wherein two of the first plurality of pointers corresponding to two of the plurality of ports are pointed to one of the second plurality of capability structures if the two ports support the same capability.

23. The computer system of claim 18, wherein the plurality of ports includes one or more Advance Switching ports.

24. The computer system of claim 18, further comprising a processor.